REMARKS

Claims 1-21, 31 and 32 are active in the above-identified application. Claims 22-30 are canceled without prejudice pursuant to applicants' election to prosecute the claims in Group I responsive to the election requirement. Claims 1-4, 11 and 18 are currently amended. Claims 31 and 32 are newly added. Claims 19 and 22-30 are canceled. No new matter is introduced therein.

Claims 1 and 2 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujii (U.S. Patent No. 4,952,523). The rejection is overcome by the amendment to claim 1. In particular, claim 1 recites, "the dielectric layer being a gate dielectric layer formed according to the standard CMOS process." Fujii does not disclose or suggest that its dielectric layer 12 is formed according to a standard CMOS process. As described in the paragraph [0030] of the specification, forming the dielectric layer as a dielectric layer according to a standard CMOS process and, thus, forming the CCD array using the standard CMOS process, provides advantages to the subject invention. In particular, the CCD imager array may be formed with other CMOS components in a single process run, allowing formation of a system-on-a-chip. Because Fujii does not disclose or suggest that its CCD imager may be formed using a standard CMOS gate dielectric layer as required by claim 1. Thus, claim 1, as amended is not subject to rejection under 35 U.S.C. § 103(a) in view of Fujii.

Furthermore, Claim 1 recites, in part, "means for stabilizing the inter-electrode gap." The Office Action's discussion of claim 1 on page 2 of the Office Action does not identify the element(s) in Fujii that meet this recitation. Referring to col. 8, lines 45-62 of Fujii, the Office Action's discussion of claim 2 on page 3 of the Office Action contends that the stabilizing means are elements 34 and 36. Applicants respectfully disagree.

First, Fujii nowhere discloses that any of its elements perform a stabilizing function. Second, the cited portions of Fujii state that regions 34 and 36 "provide virtual electrode regions." (col. 8, lines 43-46. See also, col. 8, lines 51-52, 55-56).

A virtual electrode region is different from a stabilizing region. A virtual electrode shields a portion of a cell from any gate-induced change in potential. See, col. 1, lines 8-10 and col. 2, lines 65-67 of U.S. Patent No. 4,229,752 to Hynecek incorporated by reference at page 12, lines 9-11 of the present application. On the other hand, stabilizing elements "prevent[] charge barriers from developing in the gaps and interfering with charge transfer between adjacent electrodes." (page 18, lines 23-25). The Office Action has not cited anything to show that virtual electrode regions can be considered to be a "means for stabilizing the inter-electrode gap" as defined in applicants' disclosure. Indeed, the purpose of the virtual electrode region, described above, is directly contrary to one of the stabilizing means disclosed in the subject application. At paragraph [0047] the very fields that the virtual electrode is supposed to suppress are described as a stabilizing means. Although the subject application does describe a separately doped semiconductor region as a stabilizing means, the described stabilizing means is doped in the same type as the channel, not in the opposite type as for the virtual electrode. Accordingly, claim 1 is not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii.

Claim 2 has been put into independent form by rewriting it to include the limitations of claim 1, before claim 1 was amended. The rejection of claim 2 as being unpatentable under 35 U.S.C. § 103(a) in view of Fujii is respectfully traversed. In particular, Fujii does not disclose or suggest the use of "a semiconductor region of the first conductivity type but having a different dopant concentration than the substrate, in the inter-electrode gap for stabilizing the inter-electrode gap." In the invention defined by claim 2, the channel is formed in the substrate and the "semiconductor regions of the first conductivity type" are also formed in the substrate (see paragraph [0048]). While Fujii does disclose a doped region (i.e. elements 34 and 36) between the electrodes, it is of the opposite conductivity type from the channel and, thus, does not read on the limitations of claim 2. Accordingly, claim 2 is not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii.

Claims 31 and 32, both of which depend from claim 1, have been added. Claim 31 is supported by page 9, lines 13-14. Basis in the specification for Claim 32

may be found at page 9, lines 9-17. Since these claims depend from claim 1, they are not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii for that reason alone. In addition, Fujii does not disclose the features recited in these claims because Fujii is not a charge coupled device that is made according to a standard CMOS process and using the specific CMOS structures described by these claims.

Claims 3-8, 11-13 and 18-21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Ohsawa et al. (U.S. Patent No. 5,210,433, hereinafter "Ohsawa"). Claims 3-8 depend from claim 1. The rejections overcome by the amendments to claims 1, 3, 4, 11 and 18 and by the cancellation of claim 19. As described above, claim 1 is not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii. Ohsawa concerns a method for forming a CCD array using three metallization layers (see col. 4, line 48 through col. 5, line 16). This does not conform to any standard CMOS process. Furthermore, Ohsawa does not mention the term "CMOS" anywhere in his application. Thus, the dielectric layer can not be a "gate dielectric layer formed according to the standard CMOS process" as required by amended claims 1 and 11 or a "gate oxide layer formed according to the standard CMOS process," as required by claim 18. In addition, neither Fujii, Ohsawa nor their combination discloses or suggests "at least one diffusion region in the well region of the second conductivity type forming a component of the back illuminated imager" as required by claim 20. This difference is described in greater detail below. As described above, the subject invention has advantages over the prior art because it uses a standard CMOS process. Accordingly, claims 1, 11, 18 and 20 are not subject to rejection under 35 U.S.C. § 103(a) in view of Fujii, and Ohsawa. Claims 3-8 depend from claim 1; claims 12 and 13 depend from claim 11 claim 19 depends from claim 18 and claim 21 depends from claims 18 and 20. Accordingly, these claims are not subject to rejection under 35 U.S.C. § 103(a) in view of Fujii, and Ohsawa for at least the same reasons as the claims from which they depend.

In addition, with respect to the rejection of claim 3, the Office Action acknowledges that Figures 8 and 9 of Fujii do not show a further gate electrode formed over the at least two gate electrodes and a further gate electrode overlying

the further dielectric layer and positioned over the inter-electrode gap. Therefore, the Office Action relies upon Figure 11 of Ohsawa for this structure recited in claim 3.

Claim 3, as amended, recites, in part, "a further gate electrode ... *selectively* positioned over the inter-electrode gap." Basis for this amendment may be found in Figures 7 and 8 which show the further gate electrodes 310 and 810 positioned selectively over the gaps 210.

In contrast, the "thin-film layer" 30 in Figure 7 of Ohsawa et al. is not "selectively" positioned over the inter-electrode gaps but, instead, "is insulatively disposed over the transfer control electrodes 20 to cover the layers 20 except for a formation region of the pixel photodiodes 14." The subject invention gains an advantage of reduced capacitance on the gate electrodes because the further gate electrodes are not formed over the gate electrodes but are selectively formed over the inter-electrode gaps. Thus, claim 3 is not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Ohsawa et al. for reasons independent of claim 1 from which it depends.

Because claims 4-6 depend from claim 3, they, too, are not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Ohsawa et al.

With respect to claim 7, the Office Action contends that Figure 11 of Ohsawa teaches a means for controlling gap potential. Therefore, the Office Action contends, "the combined structure of Fujii and Ohsawa inherently cause infringing fields as claimed in the gap region." Applicants respectfully disagree. Figure 11 of Ohsawa discloses the placement of gap potential control electrodes 82a et seq. (col. 8, lines 55-60). Earlier parts of Ohsawa disclose how the gap potential control electrodes are used and that a potential is applied to electrodes other than control electrodes. (col. 4, lines 48-60). Ohsawa does not disclose applying a "bias potential" to the transfer electrodes as required by claim 7. Referring to Figure 3, for example, Ohsawa discloses applying a biasing potential Vg1 to electrodes 30, not to transfer control electrodes 20. (col. 4, lines 53-56). Also, Figure 3 shows "a DC voltage control signal

... Vg1 for controlling the potential of the thin film layer 30." (col 4, lines 53-56). Therefore, Ohsawa does not disclose "means for applying respective bias potentials to the at least two gate electrodes" as recited in claim 7. For these additional reasons, claim 7 is not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Ohsawa for reasons independent of claim 1.

Even if it is assumed that bias potentials were applied to the gate electrodes (which is not conceded), Ohsawa does not disclose that such bias potentials "cause fringing fields from the at least two gate electrodes to extend into the inter-electrode gap" as recited in claim 7. The Office Action contends that Ohsawa "inherently cause[s] fringing fields as claimed in the gap region." Applicants respectfully disagree that there is any suggestion whatsoever in Ohsawa that potentials that may be applied to the gate electrodes (which is not conceded) are sufficient "to cause fringing fields from the at least two electrodes to extend into the inter-electrode gap." Moreover, it is noted that, as described above, the virtual electrode structure of Fujii is expressly for the purpose of defeating these fringing fields. Thus, Fujii can not be combined with Ohsawa to meet the limitations of claim 7.

In effect, the Office Action has concluded that it is well known (common knowledge) that the application of any potential to two gate electrodes will cause fringing fields to extend from the gate electrodes into the inter-electrode gap. Alternatively, the Office Action has taken Official Notice of the concept. The specification states that "[o]ne method for stabilizing the inter-electrode gap is to apply a suitable bias voltage to the gate electrodes 104 and so generate fringing fields that extend into and stabilize the gaps." (paragraph [0047]) There is nothing in Ohsawa suggesting that this concept is well-known or suggesting that Official Notice can be taken. Therefore, applicants respectfully object to the taking of Official Notice and ask the Examiner to cite a reference in support of the contention. See, MPEP § 2144.03.

The assertion of inherency and the implied assertion of Official Notice violates the policies outlined in the February 21, 2002 memorandum of Stephen G. Kunin, Deputy Commissioner for Patent Examination Policy. The memorandum states that

"Official notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to common knowledge in the art are capable of instant and unquestionable demonstration as being well-known." (emphasis in original). Furthermore, the memorandum states, "[i]t would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." (emphasis in original)

Since the Office Action has not cited any prior art reference in support of its inherency conclusion, claim 7 is not subject to rejection under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Ohsawa et al.

Claim 19 has been canceled. Therefore, its rejection is moot.

The rejection of claim 20 is respectfully traversed. Claim 20 recites, in part, that "the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction." The Office Action acknowledges that these features are not shown in Fujii. Nevertheless, the Office Action contends that a back illuminated imager is a conventional structure, that shielding is known in the art, and that therefore it would have been obvious to incorporate those features into Fujii. Applicants respectfully disagree.

In effect, the Office Action has taken Official Notice of these concepts without citing any supporting evidence. For the reasons pointed out above, such an unsupported rejection is improper because they are not capable of instant and unquestionable demonstration as being well-known. Applicants respectfully object to the taking of Official Notice and ask the Examiner to cite a reference in support of the contention. See, MPEP § 2144.03.

In addition, even if the recited features are well-known in the prior art, there is no suggestion in the cited prior art that the recited structure could be used as recited in claim 20.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure.* (emphasis added MPEP § 706.02(j)).

Here, the Office Action has relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or template to piece together the teachings of the prior art so that the claimed invention is rendered obvious. The Court has stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." *In re Fritch*, 23 USPQ 2d 1780, 1783, 1784 (Fed. Cir. 1992).

For the above reasons, claim 20 is not subject to rejection under 35 U.S.C. §103(a) as being unpatentable over Fujii in view of Ohsawa.

Claim 21 depends from claims 18, 19, and 20. Since those claims are allowable, claim 21 is also allowable.

Claims 16 and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Marsh et al. (U.S. Patent No. 6,196,932). These claims recite, in part, a single monolithic integrated circuit including a CCD imager array and CMOS A/D converter "coupled to receive image signals from the CCD imager array." The Office Action has relied upon hindsight gained from applicants' disclosure to reject these claims. The Office Action contends that Fujii teaches a CMOS analog to digital converter coupled to receive image signals from a CCD imager array. To the contrary, applicants have not found any disclosure in Fujii of an analog to digital converter. The Office Action also contends that since Marsh discloses a CMOS analog to digital converter, it would have been obvious to

incorporate the CMOS A/D converter from Marsh into the Fujii structure. Applicants respectfully disagree.

First, as pointed out above, Fujii does not disclose the use of any A/D converter. Therefore, the underlying basis for the combination of the references fails for that reason alone.

Second, applicants' disclosure has acknowledged that the prior art includes CCD imagers and CMOS imagers; but point out that these respective technologies have been used only for their own purposes (see paragraph [0003]). In contrast to the prior art, applicants have invented "a CCD device constructed with standard CMOS fabrication techniques" (paragraph [0002]) "by employing CCD imaging technology in a single semiconductor device manufactured using a standard CMOS fabrication process." (paragraph [0010]). As described above, the Examiner may not combine references based on hindsight gained from the subject invention. Because no reference has been cited which suggests that the two technologies can be combined, the combination can not be obvious in view of the cited references; the only motivation to combine these technologies comes from Applicants' own disclosure. The failure to find any reference that combines CCD and CMOS technologies demonstrates the accuracy of applicants' assertions in their specification and emphasizes the Office Action's reliance on hindsight to make this rejection.

Accordingly, claims 16 and 17 are not subject to rejection under 35 U.S.C. §103(a) as being unpatentable over Fujii in view of Marsh.

Applicants acknowledge with thanks the Examiner's indication that claims 9, 10, 14 and 15 would be allowable if rewritten in independent form. Applicants have not rewritten those claims in independent form at this time because they believe that their parent claims are allowable.

The prior art made of record and not relied upon is not considered any more pertinent to applicants' disclosure than the prior art already cited.

For all the foregoing reasons, applicants respectfully solicit allowance of claims 1-18, 20-21, 31 and 32.

Respectfully Submitted,

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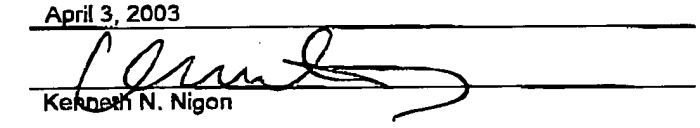

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(54) Semiconductor integrated circuit device including bipolar transistors, MOS FETs and CCD.

(57) A semiconductor integrated circuit device includes bipolar transistors (104), MOS FETs (101, 102) and a CCD (103) in and on only one semiconductor substrate (1). At least emitter electrode wiring layers (12b) of bipolar transistors (104) and one group of transfer electrode wiring layers (12a) of the CCD (103) have a stacked structure with a low resistivity which includes a first layer of doped polysilicon and a second layer of metal silicides. These electrode wiring layers are provided at the same time by successively depositing first and second layers on the semiconductor substrate and patterning the deposited layers.

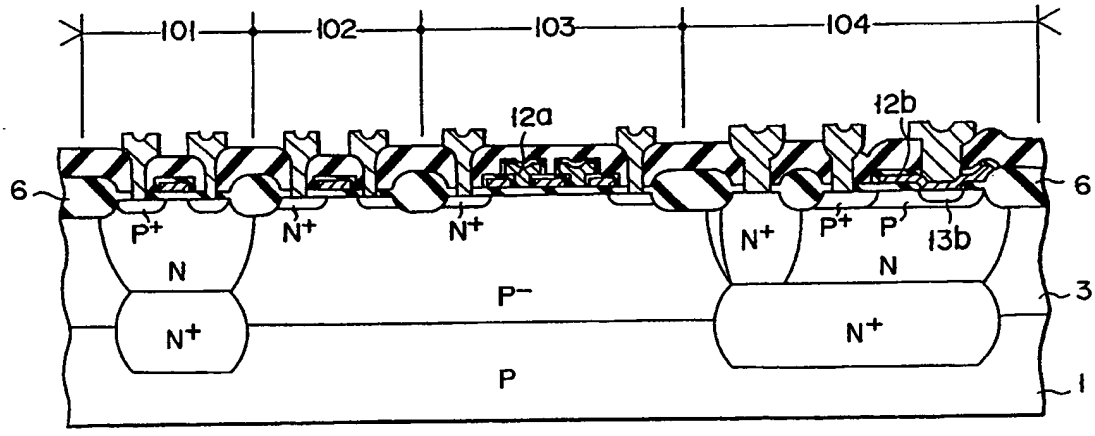

FIG. 1

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SEMICONDUCTOR INTE RATED CIRCUIT DEVICE INCLUDING BIPOLAR TRANSISTORS, MOS FETS AND CCD

This invention relates to a semiconductor integrated circuit device, and more particularly, to the so-called Bi-CMOS-CCD techniques for providing bipolar transistors, MOS type field effect transistors (MOS FETs) and a CCD device on a single semiconductor substrate.

In CCD type semiconductor devices, it is easily to increase the integration density, and also it is possible to reduce the power consumption. Therefore, they have been used as solid imagers such as line sensors and area sensors, and CCD delay line elements. For example, an IC including conventional CCD delay line elements is provided in the same semiconductor substrate together with MOS FETs. Fig. 5 is a cross-sectional view schematically illustrating elements of a conventional CCD delay line IC, wherein a CCD 403 and a CMOS FET having an N-channel MOS FET 402 and a P-channel MOS FET 401 are included in a P-type silicon substrate 41, each of the devices being isolated by a field oxide film 46. A metal electrode 56 and gate electrodes 48, 52 of the devices are interconnected to one other through electrode wiring layers, not shown, formed on an insulating film.55, thus providing a functional circuit. The CCD functions to delay signals, and the MOS FET circuits incorporated in the IC performs other associated signal processing. The capability of the MOS FET, however, is limited and signals are generally processed by an IC of the other chip having bipolar transistors.

As assembly techniques, multiple chip techniques for accommodating a plurality of chips with different functions into one package to provide one functional device have been developed.

As described above, for providing a circuit system required for the signal delay function, the CCD for performing the signal delay and the bipolar IC for carrying out most signal processing cannot be formed in one chip, and must be provided by discrete ICs. Multiple chip techniques developed for this purpose employs discrete ICs in the same manner as described above and have the following problems:

(1) Since electrodes among chips are electrically connected through bonding wires and conductive layers provided on a printed circuit board, the wiring length becomes long, so that the high speed performances of discrete ICs will not be fully exhibited.

(2) Since the package becomes large, the reliability level of the device resulting from an increase in the probability of producing cracks due to an increased number of pellets, the deterioration of humidity resisting property, etc., may be lowered.

(3) Since discrete ICs are used, it may be difficult to provide an optimum system. It may also be difficult to reduce the device size by decreasing the number of pins. In addition, there is a limit to reduce the power consumption of the device.

Relating to the ICs themselves including at least one CCD type device and CMOS FETs, the MOS type transistor in general has a poor driving ability and is not good at the analogue signal processing. The MOS type analogue circuit decreases the yield of ICs.

As has been described above, in the conventional semiconductor integrated circuit device comprised of the CCD type IC, bipolar type ICs and MOS type ICs, a plurality of discrete ICs or LSIs are combined to provide one functional system. Therefore, the prior art techniques involves the decrease in the high speed performance due to bonding wires, the decrease in the reliability level, the difficulty in obtaining the system ICs and limits in reducing the device size and the power consumption due to the large package, and the decrease in the yield due to MOS type analogue circuits.

Further, it has been generally required to provide semiconductor integrated circuit devices having multifunctions and high speed operation. Accordingly, for example, it have been ordinary required to reduce the electrode wiring resistance and to increase the integration density.

Accordingly, an object of the present invention is to provide a semiconductor integrated circuit device wherein bipolar transistors, MOS FETs and a CCD are provided in one semiconductor chip, thereby eliminating the aforesaid problems associated with prior art techniques.

Another object of the invention is to provide a semiconductor integrated circuit device having the high speed operation.

A still further object of the invention is to provide a method for making the semiconductor integrated circuit device without using a complicated process.

According to one aspect of the invention, there is provided a semiconductor integrated circuit device which includes bipolar transistors, MOS FETs and a CCD in and on only one semiconductor substrate. At least emitter electrode wiring layers of the bipolar transistors and one group of transfer electrode wiring layers of the CCD have a stacked structure with a low resistivity which includes a first

layer of doped polysilicon and a second layer of metal silicides. These electrode wiring layers are provided at the same time by successively depositing first and second layers on the semiconductor substrate and patterning the deposited layers.

According to another aspect of the present invention, there is provided a method of making the semiconductor integrated circuit device according to a principle incorporated in the firstly referred aspect of the present invention.

The novel and distinctive features of the invention are set forth in the claims appended to the present application. The invention itself, however, together with further objects and advantages thereof may best be understood by reference to the following description and accompanying drawings, in which:

Fig. 1 is a cross-sectional view schematically illustrating a semiconductor integrated circuit device according to a first embodiment of the invention;

Figs. 2A and 2B are cross-sectional views showing electrode wiring structures used as emitter electrode wiring layers of bipolar transistors, and as at least one of gate electrode wiring layers of MOS FETs and those of a CCD, in the semiconductor integrated circuit device of Fig. 1;

Figs. 3A to 3D are cross-sectional views schematically illustrating a process for making the semiconductor integrated circuit device of Fig. 1;

Fig. 4 is a cross-sectional view of a semiconductor integrated circuit device according to a second embodiment of the invention; and

Fig. 5 shows a cross-sectional view schematically showing a prior art semiconductor integrated circuit device.

A semiconductor integrated circuit device according to the first embodiment of the invention will be described with reference to Fig. 1.

In the figure, a P-channel MOS FET 101, an N-channel MOS FET 102, a CCD 103 with a two-layer gate structure and a bipolar transistor 104 are formed on a semiconductor substrate 1 including a P-type epitaxial layer 3 and a P-type silicon substrate 1. Each element of the device is isolated through a field oxide film 6. An emitter electrode wiring layer 12b of the bipolar transistor 104 and a second group of transfer electrode wiring layers 12a of the CCD 103 are formed of a polysilicon layer (As-doped) $12'$ and a silicide layer ($MoSi_2$) $12''$ which are patterned using the same process as shown in Figs. 2A and 2B. An N^+-type emitter diffused layer 13b of the bipolar transistor 104 is a shallow layer formed by using the emitter electrode wiring layer 12b as an impurity diffusion source.

Referring to Figs. 3A to 3D, a method of making the device shown in Fig. 1 will now be described together with a detailed structure of the device.

An N^+-type buried layer 2 is formed in the P-type silicon substrate 1 having a resistivity of the order of 18-25 Ω.cm by solid phase diffusion of antimony (Sb), followed by growing a boron-doped P-type epitaxial layer 3 to a thickness of about 3 μm thereon. By selective ion implantation and thermal diffusion, an N-type well layer 4 and a deep N^+-type layer 5 with a high concentration are then provided, followed by forming a field oxide film 6 by selective oxidation techniques (LOCOS) for providing an isolation structure. (Fig. 3A)

After the oxide film is once removed from the substrate surface, a first gate oxide film 7 having a thickness of 500 to 700 A is formed on the substrate by the thermal oxidation technique at 950° C. Using a resist layer as a mask, the P^--type epitaxial layer 3 is subjected to ion implantation to provide both a buried channel region for the CCD and channel regions for MOS FETs, respectively. An undoped polysilicon layer is subsequently deposited to a thickness of 4,000 Å followed by diffusing phosphorous at 950° C thereinto. The doped polysilicon layer is patterned to form gate electrode wiring layers 8a of the MOS FETs and a first group of transfer electrode wiring layers 8b of the CCD. A multilevel structure comprised of a doped polysilicon layer and a silicide layer or a high melting metal layer is used as the electrode wiring layer. Using the first group of transfer electrode wiring layers 8b and a resist layer, ion implantation is performed to provide a barrier of the CCD. (Fig. 3B)

The exposed oxide film is removed by wet etching except for portions underneath the electrode wiring layers 8a and 8b. A second gate oxide film 9 is formed over the substrate surface at 950° C by the thermal oxidation technique. Boron ions are selectively implanted into the N-type well region to provide a base region 10 of the bipolar transistor 104, using a resist layer as a mask. A window for making an emitter region in the base region 10 is formed in the oxide film 9, and a polysilicon layer is deposited on the substrate surface to a thickness of the order of 1,000 Å. Thereafter, Arsenic (As) ions are implanted into the polysilicon layer at a dose of 4×10^{15} atoms/cm^2. Covering the doped polysilicon layer with a CVD film such as SiO_2, the impurity of As is diffused into the base region. For doping the polysilicon layer with an impurity, the ion implantation described above may be replaced by the use of a diffusion source of POCℓ3 or the like, or by the deposition of a doped polysilicon. The CVD film is then removed, and a silicide of a high melting metal, for example, $MoSi_2$, is sputtered onto the polysilicon layer to a thickness of 2,500 A. The

resultant layer is patterned to provide a second group of transfer electrode wiring layers 12a of the CCD and the emitter electrode wiring layer 12b of the bipolar transistor. (Fig. 3C)

Next, arsenic (As) ions are implanted into the P--type epitaxial layer to provide both N^+-type regions of CCD 103 and N^+-type source and drain regions of the N-channel MOS FET 102, and the substrate is subjected to thermal oxidation. Boron ions are selectively implanted into the N-type well region and the base region 10 to form and drain regions of the P-channel MOS FET 101 and an external base region of the bipolar transistor 104. The ion implantation process is carried out by a self-alignment techniques using the field oxide film 6, the electrode wiring layers 8a, 8b and the emitter electrode wiring layer 12b as masks. Therefore, the distance between the external base region and the emitter region may be reduced to provide bipolar transistors having the high integration density and high speed operation.

After a CVD film (SiO_2) having a thickness of about 3,000 Å, a BPSG film having a thickness of about 9.000 Å, and a PSG film having a thickness of about 2,500 Å, the successively deposited on the substrate surface, the resultant structure is melted at 950°C to perform the phosphorus gettering and the impurity diffusion for the emitter at the same time, thereby providing N^+-type diffused layers 13a of the N-channel MOS FET 102 and the CCD 103, the N^+-type emitter diffused layer 13b of the bipolar transistor 104, P^+-type diffused layers 14a of the P-channel MOS FET 101, and an external base region 14b of the bipolar transistor. In the formation of the N^+-type emitter diffused layer 13b, the N^+-type collector diffused layer 5 may be subjected to the similar treatment. Thereafter, known metallization processes are applied to the resultant structure to form metal electrode wiring layers 16, thereby completing a semiconductor integration circuit device. In this case, reference numeral 15 designates an interlevel insulator composed of the CVD film, the BPSG film and the PSG film. (Fig. 3D)

In the foregoing embodiment, the emitter electrode wiring layer 12b of the bipolar transistor and the second group of transfer electrode wiring layers 12a of the CCD, which have the two-layer structure, are patterned in the same process, but the invention is not limited to it. For example, the first group of transfer electrode wiring layers of the CCD and the emitter electrode wiring layer of the bipolar transistor may be patterned in the same process. More specifically, the emitter electrode wiring layer of the bipolar transistor and at least one of the electrode wiring layers of the MOS FETs and the CCD may be patterned in the same process.

Accordingly, in the case of a CCD with one-transfer electrode structure, all of the gate electrode wiring layers of the MOS FETs and the emitter electrode wiring layers of the bipolar transistors may be patterned in the same process. Fig. 4 is a cross-sectional view showing another embodiment of an integrated circuit device in this instance. A CCD 303 in the figure has one-electrode structure. The transfer electrode wiring layers 32a of the CCD, gate electrode wiring layers 32a of the P- and N-channel MOS FETs 301 and 302, and the emitter electrode wiring layers 32a of the bipolar transistor 304 are formed of a doped polysilicon layer and a silicide layer to provide an electrode wiring structure, which is patterned at the same time. In this case, the gate electrode wiring layers of the MOS FETs and the CCD are completed by only one process, so that the device may be easily produced.

Since each of the electrode wiring layers in the embodiment is comprised of the doped polysilicon layer and the silicide layer, the resistivity may be lowered to about 3 Ω/□ . The electrode material is not limited to such a composite layer. Low resistivity electrode wiring layers may be similarly obtained using the doped polysilicon layer and another high melting metal layer.

According to the semiconductor integrated circuit device of the present invention, the following advantages will be provided since at least one CCD type device, bipolar transistors and MOS FETs are integrally formed in one semiconductor chip.

(1) Since electrical connections among the elements of the devices are performed by the electrode wiring layers in place of conventional conductive layers in printed circuit boards or bonding wires, the high speed performance can be improved.

(2) Since the device is provided by only one chip unlike the prior art techniques using a plurality of chips to be arranged in one package, the probability of generating unwanted troubles such as cracks, deterioration of humidity resisting property, etc., may be reduced to improve the reliability level.

(3) Since the layout pattern of the functional elements provided on the epitaxial layer is occasionally changed without complicated processes, an optimum layout pattern corresponding to a desired system function can be selected to obtain desired system ICs. Further, since the analogue signal processing is carried out by the bipolar IC, MOS IC suitable for decreasing the power consumption can be put to practical use. Accordingly, the lowering of the yield caused by the use of MOS type analogue circuits can be improved. Still further, it is possible to reduce the device size by decreasing the number of pins.

The emitter electrode wiring layers of the bipolar transistors and the electrode wiring layers of the CCD and the MOS type ICs are formed of the low resistivity layers. The high speed operation of the device can be greatly improved. Since the bipolar transistors have the shallow emitters and the reduced distance between the external base and the emitter, transistors adapted to the high speed operation can be provided. Yet, use of the electrode wiring layers may achieve the high integration density of electronic circuits.

As has been described in detail, since bipolar transistors, MOS FETs and at least one CCD are provided in the one chip and the low resistivity materials are used as the electrode wiring layers of the function elements, the problems associated with prior art techniques will be eliminated to attain the high speed operation, the high system integration and the low power consumption. Accordingly, semiconductor integrated circuit devices having high reliability will be provided with high yield.

It is further understood by those skilled in the art that the foregoing description is preferred embodiments of the disclosed device and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor integrated oircuit devioe including MOS type field effect transistors (101, 102) with gate electrode wiring layers and at least one charge coupled device (103) having at least one group of transfer electrode wiring layers (12a), which are provided in one conductivity type semiconductor substrate (1) having opposite conductivity type well regions (4) and which are isolated through a field oxide film (6) from one another,
characterized in that bipolar transistors (104) with emitter electrode wiring layers (12b) are provided in said well regions (4), and that at least said emitter electrode wiring layers (12b) and said transfer electrode wiring layers (12a) are comprised of an electrode wiring structure including a first layer of doped polysilicon and a second layer selected from high melting materials.

2. The device according to claim 1,
characterized in that said second layer is composed of a metal silicide.

3. The device according to claim 1,
characterized in that said second layer is composed of a high melting metal.

4. The device according to claim 1,
characterized in that electrode wiring structure is applied to said gate electrodes.

5. The device according to claim 1,
characterized in that each of said bipolar transistors (104) has a shallow emitter region (13b).

6. The device according to claim 1,
characterized in that said MOS type field effect transistors include P- and N-channel MOS FETs (101, 102).

7. The device according to claim 1,
characterized in that said bipolar transistors (104) provide analogue circuits.

8. A method of making a semiconductor integrated circuit device including bipolar transistors (104) with emitter electrode wiring layers (12b), MOS type field effect transistors (101, 102) with gate electrode wiring layers (8a) and at least one charge coupled device (103) having at least one group of transfer electrode wiring layers (8b, 12a), which are provided in a semiconductor substrate (1) having both well regions (4) and a field oxide film (6) for defining isolated regions,
characterized by:
forming a first oxide film (7) on said semiconductor substrate (1);
depositing a conductive layer on said isolated regions;
patterning said conductive layer to provide both gate electrode wiring layers (8a) for MOS FETs (101, 102) and a first group of transfer electrode wiring layers (8b) for at least one of charge coupled device (103) at the same time;
selectively removing said first oxide film (7) from said semiconductor substrate;
forming a second oxide film (9) over said semiconductor substrate to cover said gate electrode wiring layers and said first group of transfer electrode wiring layers therewith;
selectively introducing an impurity into said well regions (4) to provide base regions (10) for bipolar transistors therein;
successively depositing a doped polysilicon layer and a layer of high melting materials on both said isolated regions for said charge coupled device (103) and said base regions (10) for said bipolar transistors;
patterning said layers to provide both a second group of transfer electrode wiring layers (12a) for said charge coupled device and emitter electrode wiring layers (12b) for said bipolar transistors at the same time; and
selectively introducing an impurity into said isolated regions for said MOS FETs to provide source and drain regions thereof.

9. The method according to claim 8,
characterized in that one conductivity type epitaxial layer (3) with a low impurity concentration is grown on a semiconductor substrate (1).

10. The method according to claim 8,

characterized in that said conductive layer is composed of a doped polysilicon layer.

11. The method according to claim 8, characterized in that said conductive layer is composed of a doped polysilicon film and a film of high melting materials.

12. The method according to claim 11, characterized in that said high melting materials are selected from high melting metals and their silicides.

13. The method according to claim 8, characterized in that the impurity contained in said doped polysilicon layer is diffused into said well regions to form emitter regions (13b) in said base regions (10).

14. A method of making a semiconductor integrated circuit device including bipolar transistors (304) with emitter electrode wiring layers (32a), MOS type field effect transistors (301, 302) with gate electrode wiring layers (32a) and at least one charge coupled device (303) having transfer electrode wiring layers (32a), which are provided in a semiconductor substrate having both well regions and a field oxide film for defining isolated regions, characterized by:

forming an oxide film on said semiconductor substrate;

selectively introducing an impurity into said well regions to provide base regions for said bipolar transistors (304) therein;

successively deposing a doped polysilicon layer and a layer of high melting materials above said semiconductor substrate;

patterning said layers to provide emitter electrode wiring layers (32a) for said bipolar transistors, gate electrode wiring layers (32a) for said MOS FETs, and transfer electrode wiring layers (32a) for said charge coupled device at the same time; and

selectively introducing an impurity into said isolated regions for said MOS FETs to provide source and drain regions thereof.

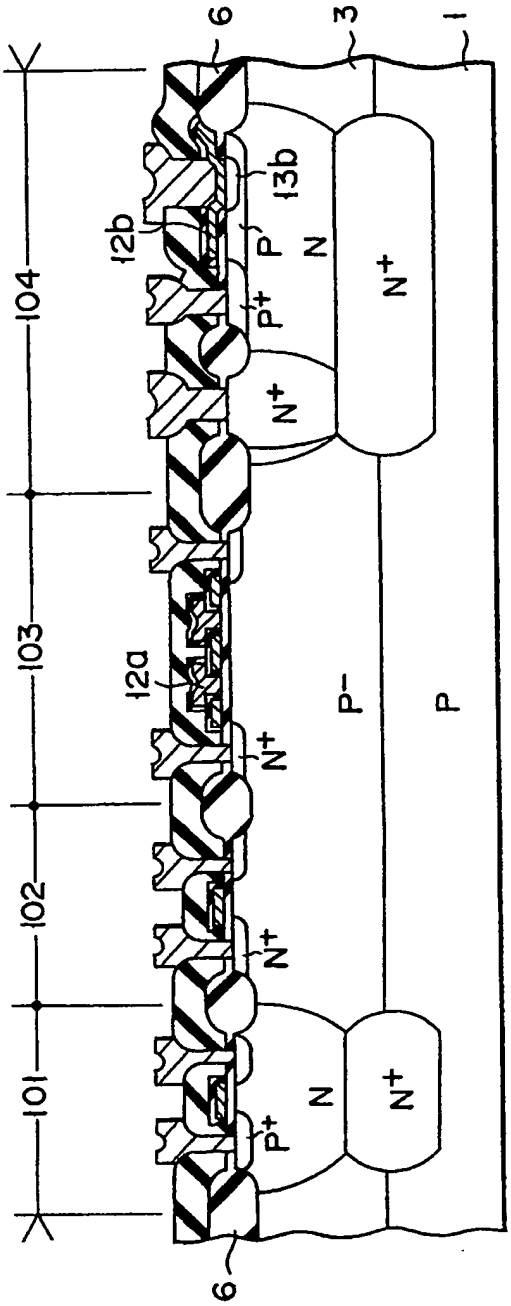

FIG. 1

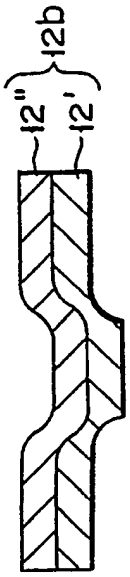

FIG. 2B

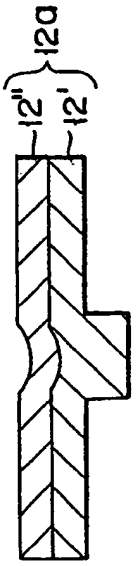

FIG. 2A

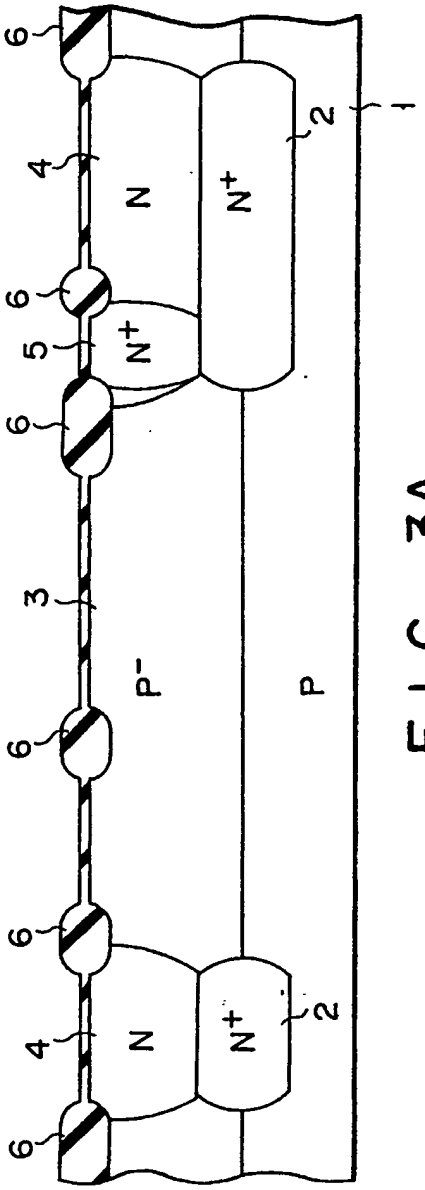

FIG. 3A

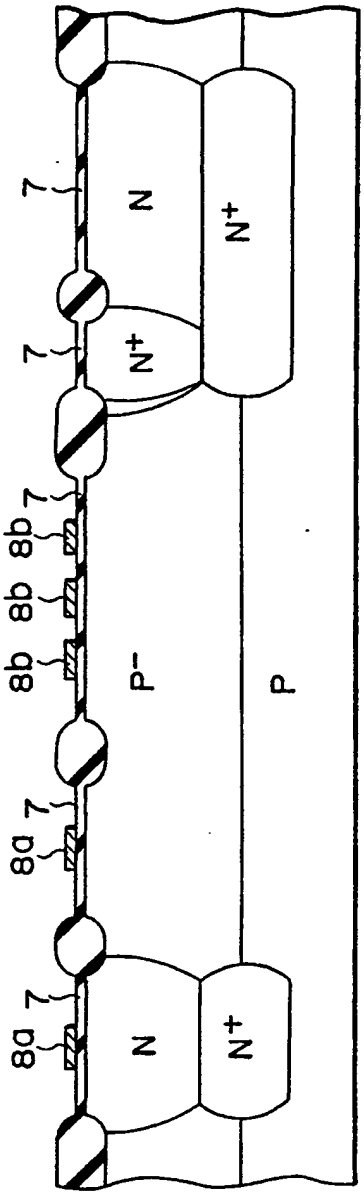

FIG. 3B

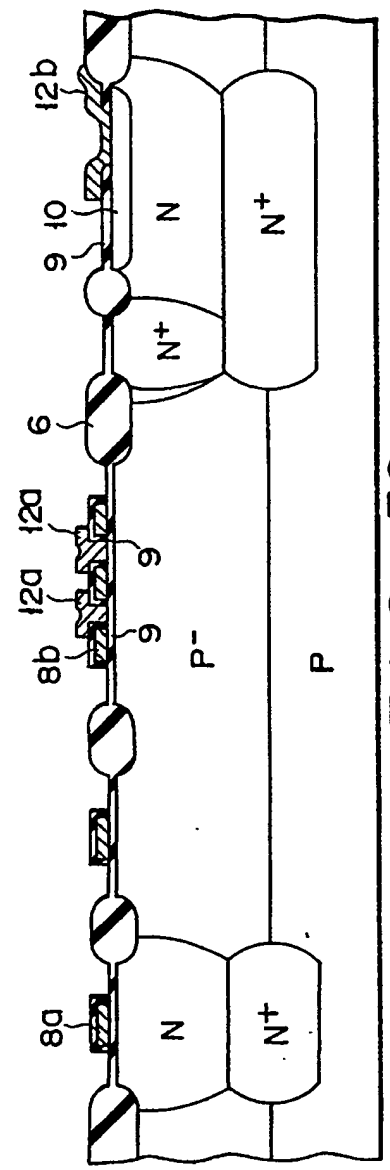
12b
10
9
N
N+
6
12c
12a
9
8b
9
P-
P
8a
N
N+

FIG. 3C

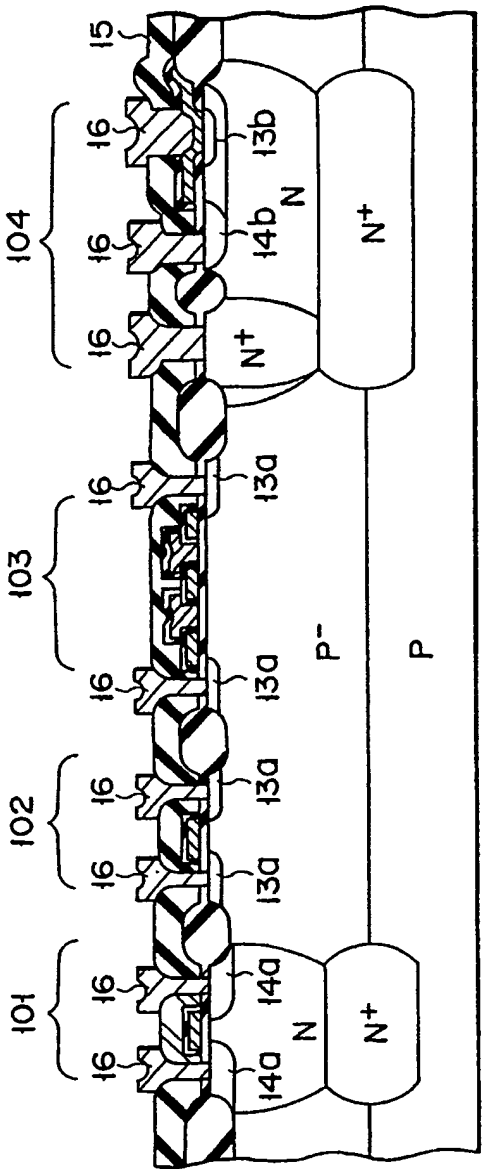
15
16
13b
104
16
14b
N
N+
16
N+
16
13a
103
16
13a
P-
P
16
13a
102
16
13a
101
16
14a
N
N+
16
14a

FIG. 3D

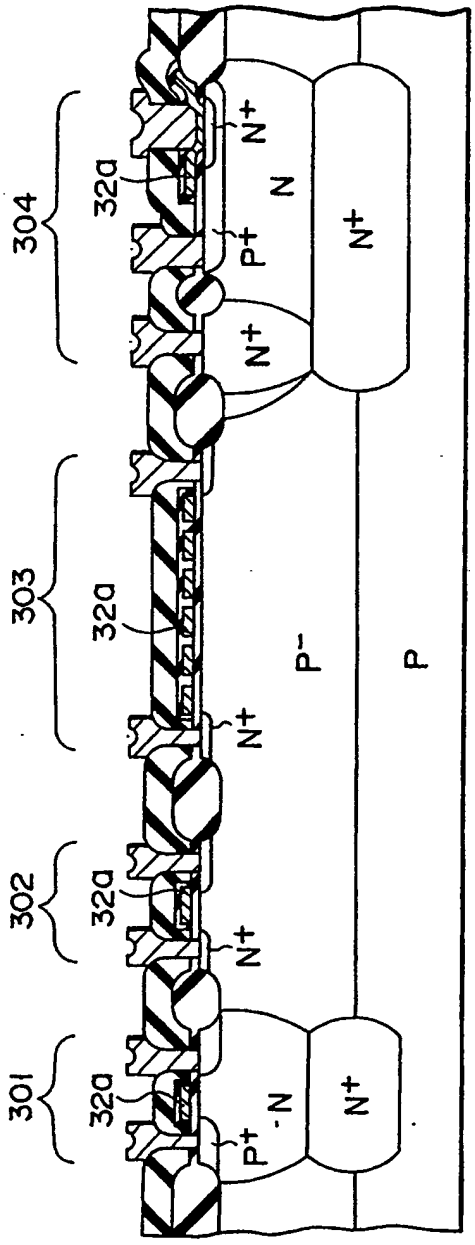

FIG. 4

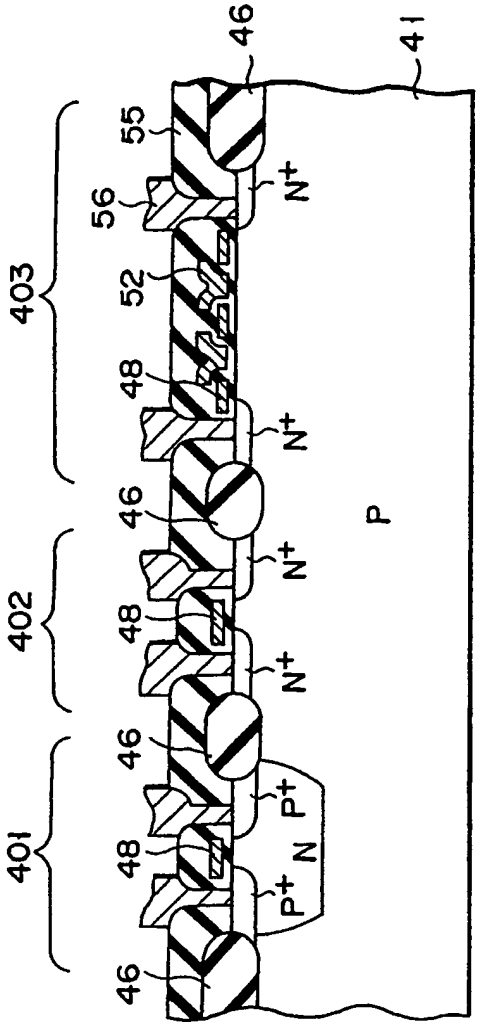

FIG. 5